Description

HY5171 is a 280kHz switching regulators with a high efficiency, 1.5A integrated switch. These parts operate over a wide input voltage range, from 2.7V to 30V. The flexibility of the design allows the chips to operate in most power supply configurations, including boost, flyback, inverting, and SEPIC. HY5171 utilize current mode architecture, which allows excellent load and line regulation, as well as a practical means for limiting current. The circuit design includes provisions for features such as frequency synchronization, shutdown, and feedback controls for either positive or negative voltage regulation.

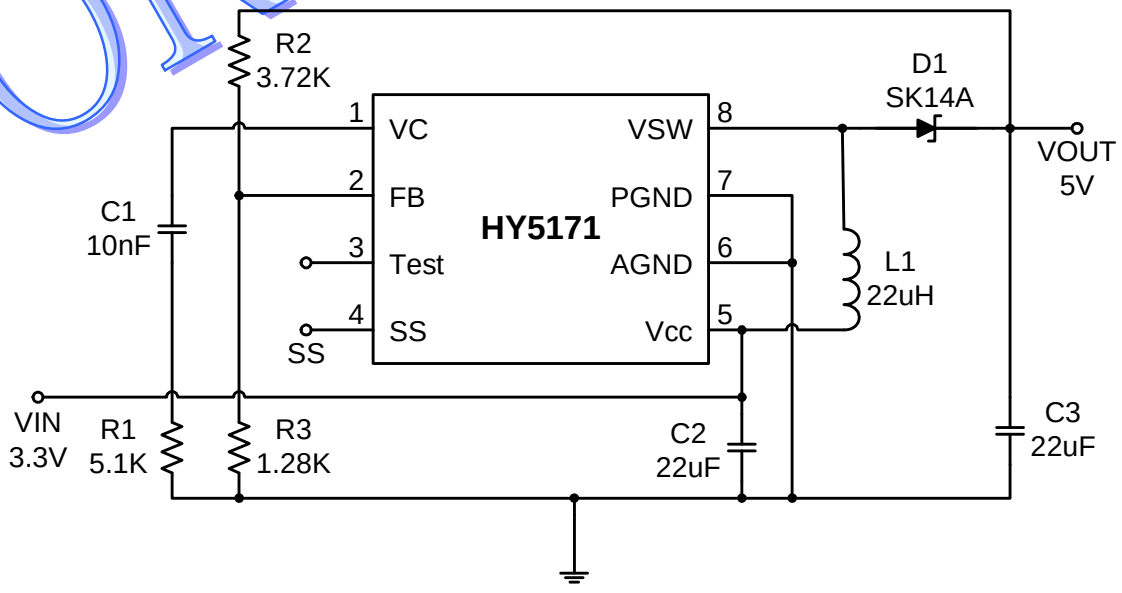
Features

- Integrated Power Switch 1.5A.
- 2.7V to 30V input Range.
- Minimum External Components..
- External Synchronization.
- Built in Over Current Protection.
- Thermal Shutdown with Hysteresis.
- Regulates Positive or Negative output voltage.
- Standby Current is less than 50uA.

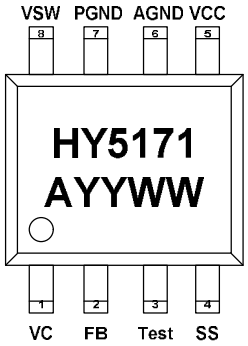
Applications

- Step-Up Regulators.
- CCFL backlighting driver.
- Laptop Computer Supplies.
- Multi-Output Flyback Supplies.
- Inverting Supplies.
- TFT LCD Bias Supplies.

Typical Applications Circuit



Marking Information & Pin Configuration

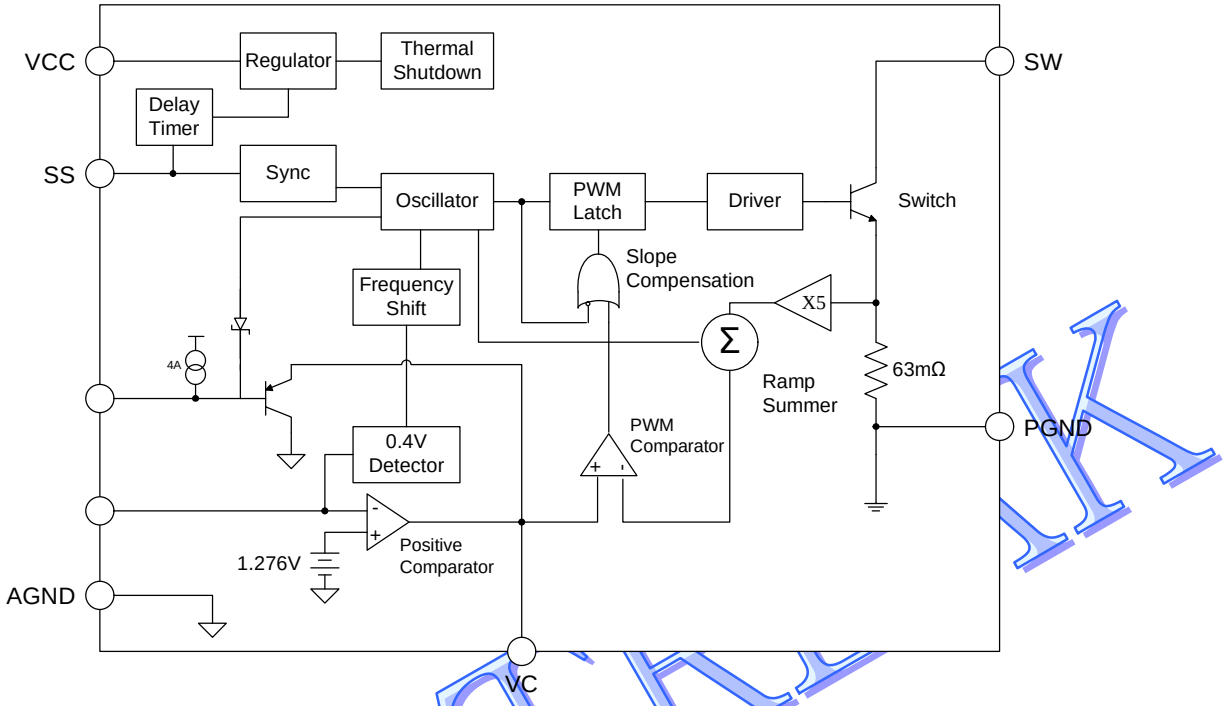


A : Assembly Information
YY : Year
WW : Weekly

Pin Definition

PIN NUMBER	PIN SYMBOL	PIN DESCRIPTION
1	VC	Loop compensation pin of the error amplifier. It can be implemented by a simple RC as shown in the application diagram on page1 as R1 and C1.
2	FB	Regulator feedback pin. It senses a positive output voltage and reference to 1.276V. When the voltage of it falls below 0.4V, operation frequency will be reduced to 20% of the nominal frequency.
3	Test	Internal logic test pin, it should be left floating or tied to ground. Connection to a voltage between 9.5V and 15V shuts down the internal oscillator.
4	SS	Synchronization pin. The pin is used to synchronize the part to nearly twice the base frequency. A TTL low shut the part down and put it into low current mode. If synchronization is not used, it should be tied to high or left it floating for normal operation.
5	VCC	Input power supply.
6	AGND	Analog ground.
7	PGND	Power ground.
8	VSW	Pin VSW is internal power switch. The open voltage across the power switch can be as high as 40V. To minimize radiation, use a trace as short as practical.

Block Diagram



ABSOLUTE MAXIMUM RATINGS

RATING	VALUE	UNIT
IC Input (VCC), Shutdown/Sync (SS)	-0.3 to 30	V
Loop Compensation (VC), Test Pin (Test)	-0.3 to 6	V
Voltage Feedback Input (FB)	-0.3 to 10	V
Switching Pin (VSW)	-0.3 to 40	V
Junction Temperature Range	-40 to 150	℃
Storage Temperature Range	-65 to 150	℃
Thermal Impedance: SOP-8	128	˚C/W
Continuous Power Dissipation TA =+25˚C : SOP-8	830	mW
ESD Protection HBM	1200	V

ELECTRICAL CHARACTERISTICS

(TA = 25°C, UNLESS OTHERWISE SPECIFIED)

Error Amplifier

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
FB Reference Voltage	VC tie to FB, Measure at FB	1.246	1.276	1.300	V
FB Input Current	FB=VREF	-0.1	0.1	1.0	μA
FB Reference Voltage Line Regulation	VC=FB	-	0.01	0.03	%/V
Error Amplifier Transconductance	IVC=25μA	300	550	800	μMho
Error Amplifier Gain	Note 1.	200	500		V/V
Negative Error Amplifier Gain	Note 1.	100	180	320	V/V
VC Source Current	FB=1.0V, VC=1.25V	25	50	90	μA
VC Sink Current	FB=1.5V, VC=1.25V	200	625	1500	μA
VC High Clamp Voltage	FB=1.0V, VC Source 25μA	1.5	1.7	1.9	V
VC Low Clamp Voltage	FB=1.0V, VC Sink 25μA	0.25	0.5	0.65	V
VC Threshold	Reduce VC from 1.5V until switching stop	0.75	1.05	1.3	V

Oscillator

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Base Operating Frequency	FB=1.0V	230	280	310	KHz
Reduced Operating Frequency	FB=0V	30	52	120	KHz
Maximum Duty Cycle	-	90	94		%
FB Frequency Shift Threshold	Frequency drops to reduced operating frequency	0.36	0.4	0.44	V

Sync / Shutdown

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Sync Range	-	320	-	500	KHz
Sync Pulse Transition Threshold	Rise time = 20nS	2.5			V
SS Bias Current	SS=0V SS=3.0V	-15 -	-3.0 3.0	- 8.0	μA
Shutdown Threshold	-	0.5	0.85	1.2	V
Shutdown Delay	2.7V ≦ VCC ≦ 12V 12V < VCC ≦ 30V	12 12	80 36	350 200	μS

Power Switch

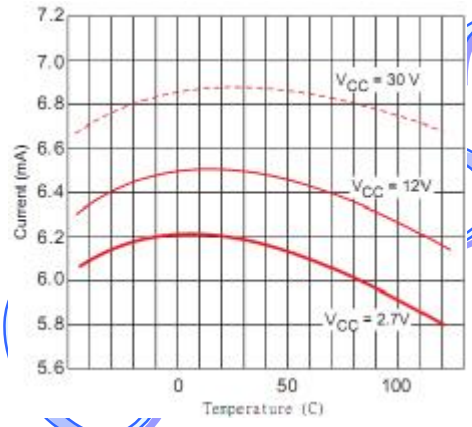
PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Switch saturation Voltage	I_{SWITCH} = 1.5A (Note 1.) I_{SWITCH} = 1.0A, 0°C≦TC≦85°C I_{SWITCH} = 1.0A, -40°C≦TA≦0°C(Note 1.) I_{SWITCH} = 10mAA	-	0.8 0.55 0.75 0.09	1.3 1.0 1.3 0.45	V
Switch Current limit	50% Duty cycle (Note 1.) 80% Duty cycle (Note 1.)	1.6 1.5	1.9 1.7	2.4 2.2	A
Minimum Pulse Width	FB=0V, I_{SW}=4.0A(Note 1.)	200	250	300	nS
$\Delta I_{CC}/\Delta V_{SW}$	2.7V ≦ VCC ≦ 12V, 10mA ≦ I_{SW} ≦ 1.0A 12V < VCC ≦ 30V, 10mA ≦ I_{SW} ≦ 1.0A 2.7V ≦ VCC ≦ 12V, 10mA ≦ I_{SW} ≦ 1.0A(Note 1.) 12V < VCC ≦ 30V, 10mA ≦ I_{SW} ≦ 1.0A	-	10 - 17 -	30 100 30 100	mA/A
Switch Leakage	VSW=40V, VCC=0V	-	2.0	100	μA

General					
PARAMETER	**CONDITION**	**MIN**	**TYP**	**MAX**	**UNIT**
Operating Current	ISW = 0	-	**5.5**	**8**	mA
Shutdown Mode Current	2.7V ≦ VCC ≦ 12V, VC<0.8V, SS=0V 12V < VCC ≦ 30V, VC<0.8V, SS=0V	-	**12** -	**60** **100**	μA
Minimum Operation Input Voltage	VSW Switching, maximum I_{SW} = 10mA		**2.45**	**2.7**	V
Thermal Shutdown	(Note 1.)	**150**	**180**	**210**	°C
Thermal Hysteresis	(Note 1.)		**25**		°C

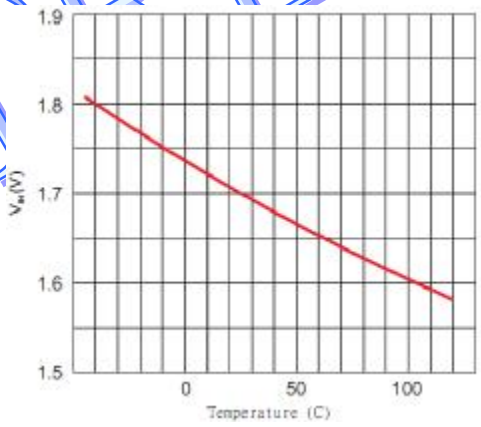
Note

1. Guaranteed by design, not 100% tested in production.

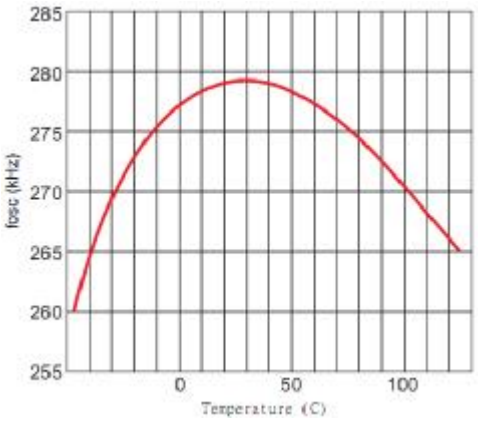
PERFORMANCE CHARACTERISTICS



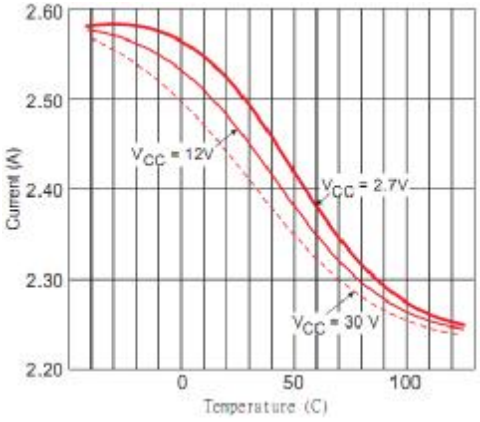
ICC vs. Temperature



Minimum Input Voltage vs. Temperature



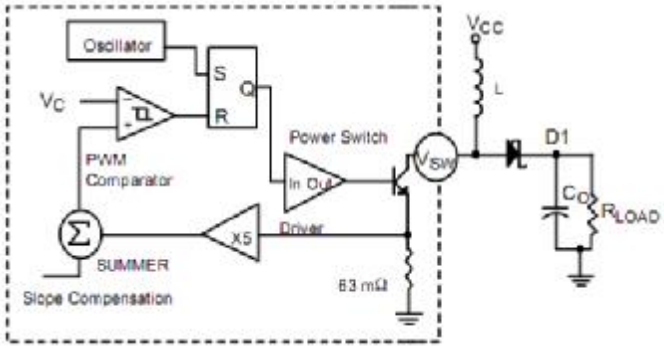
Switching Frequency vs. Temperature



Current Limit vs. Temperature

APPLICATION INFORMATION

Current Mode Control

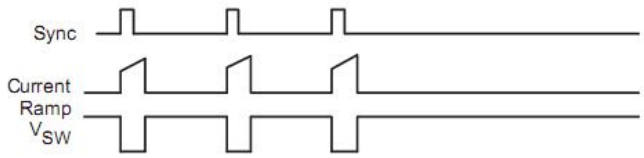


Current Mode Control Scheme

The HY5171 incorporates a current mode control scheme. In which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on-time power switch. The oscillator is used as a fixed-frequency clock to ensure a constant operational frequency. The resulting control scheme features several advantages over conventional voltage mode control. First, derived directly from the inductor, the ramp signal responds immediately to line voltage changes. This eliminates the delay caused by the output filter and error amplifier, which is commonly found in voltage mode controllers. The second benefit comes from inherent pulse-by pulse current limiting by merely clamping the peak switching current. Finally, current mode commands an output current rather than voltage, and then the filter offers only a single pole to the feedback loop. This allows both a simpler compensation and a higher gain-band width over a comparable voltage mode circuit.

Without discrediting its apparent merits, current mode control comes with its own peculiar problem and mainly sub-harmonic oscillation at duty cycles over 50%. The HY5171 solves this problem by adopting a slope compensation scheme, in which, a fixed ramp generated by the oscillator is added to the current ramp. A proper slope rate is provided to improve circuit stability without sacrificing the advantages of current mode control.

Oscillator and Shutdown



Timing Diagram of sync and shutdown

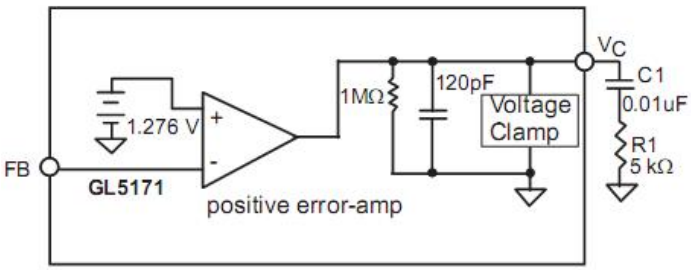
The oscillator is trimmed to guarantee 18% frequency accuracy. The output of the oscillator turns on the power switch at a frequency of 280kHz, as shown in figure "Current Mode Control Scheme". The power switch is turned off by the output of the PWM comparator.

A TTL compatible sync input at the SS pin is capable of syncing up to 1.8 times the base oscillator frequency. As shown in above figure" Timing Diagram of sync and shutdown", in order to sync to a higher frequency, a positive transition turns on the power switch before the output of the oscillator goes high, thereby resetting the oscillator. The sync operation allows multiple power supplies to operate at the same frequency.

A sustained logic low at the SS pin will

shutdown the IC and reduce the supply current. An additional feature includes frequency shift to 20% of the nominal frequency when the FB pin trigger the threshold. During power up, overload, or short circuit conditions, the minimum switch on-time is limited by the PWM comparator minimum pulse width. Extra switch off-time reduces the minimum duty cycle to protect external components and the IC itself. As previously mentioned, this block also produces a ramp for the slope compensation to improve regulator stability.

Error Amplifier



Error Amplifier Equivalent Circuit

The FB pin is directly connected to the inverting input of the positive error amplifier, whose non-inverting input is fed by the 1.276V reference. The amplifier is transconductance amplifier with a high output impedance of approximately 1MΩ, as shown in figure "Error Amplifier Equivalent Circuit". The VC pin is connected to the output of the error amplifier and is internally clamped between 0.5V and 1.7V. A typical connection at the VC pin includes a capacitor in series with a resistor to ground, forming a pole/zero for loop compensation.

An external shunt can be connected between the VC pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

Switch Driver and Power Switch

The switch driver receives a control signal from the logic section to drive the output power switch. The switch is grounded through emitter resistors (63mΩ total) to the PGND pin. PGND is not connected to the IC substrate so that switching noise can be isolated from the analog ground. The peak switching current is clamped by an internal circuit. The clamp current is guaranteed to be greater than 1.5A and varies with duty cycle due to slope compensation. The power switch can withstand a maximum voltage of 40V on the collector (VSW pin). The saturation voltage of the switch is typically less than 1V to minimize power dissipation.

Short Circuit Condition

When a short circuit condition happens in a boost circuit, the inductor current will increase during the whole switching cycle, causing excessive current to be drawn from the input power supply. Since control ICs don't have the means to limit load current, an external current limit circuit (such as a fuse or relay) has to be implemented to protect the load, power supply and ICs. In other topologies, the frequency shift built-in to the IC prevents damage to the chip and external components. This feature reduces the minimum duty cycle and allows the transformer secondary to absorb excess energy before the switch turns back on.

HY5171 can be activated by either connecting the VCC pin to a voltage source or by enabling the SS pin. When the VCC voltage is

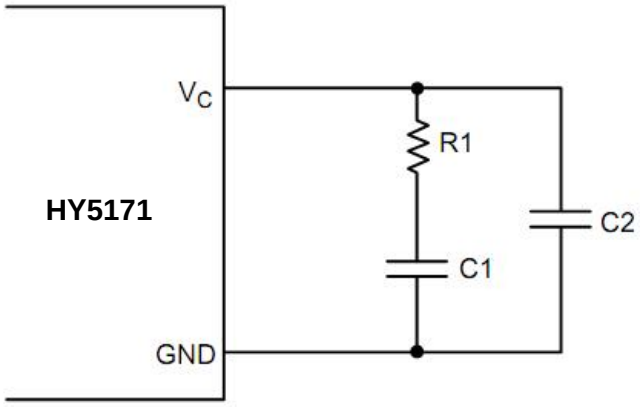
below the minimum supply voltage, the VSW pin is in high impedance. Therefore, current conduces directly from the input power source to the output through the inductor and diode. Once VCC reaches approximately 1.5V, the internal power switch briefly turns on. This is a part of HY5171's normal operation. The turn-on of the power switch accounts for the initial current swing.

When the VC pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the VSW pin. Detecting a low output voltage at the FB pin, the built-in frequency shift feature reduces the switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on-time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull–on, by which the sink current of the error amplifier is increased once an over-voltage condition is detected. The over-voltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

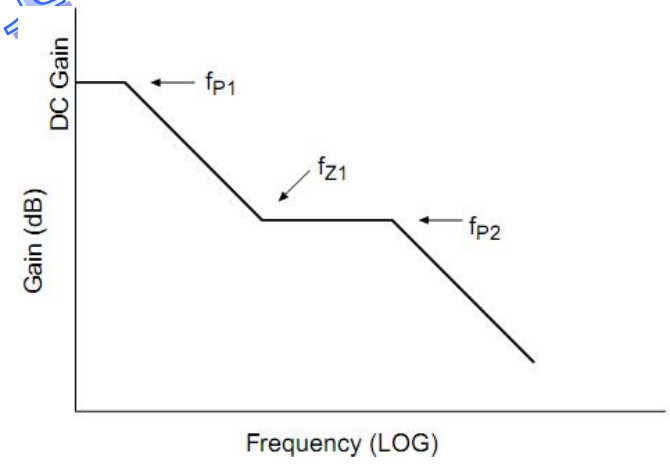
COMPONENT SELECTION

Frequency Compensation



Typical Compensation Network

The goal of frequency compensation is to achieve desirable transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in figure "Typical Compensation Network", provides a frequency response of two poles and one zero. This frequency response is further illustrated in the Bode plot shown in figure "Bode Plot of the Compensation Network".



Bode Plot of the Compensation Network

The high DC gain in figure "Bode Plot of the Compensation Network" is desirable for achieving DC accuracy over line and load variations. The DC gain of a transconductance

error amplifier can be calculated as follows:

$$\mathbf{Gain_{DC} = G_M \times R_O}$$

where:

G_M = error amplifier transconductance;

R_O = error amplifier output resistance ≈ 1 MΩ.

The low frequency pole, fP1, is determined by the error amplifier output resistance and C_1 as:

$$fp1 = \frac{1}{2p\,C_1 R_O}$$

The first zero generated by C_1 and R_1 is:

$$fZ1 = \frac{1}{2p\,C_1 R_1}$$

The phase lead provided by this zero ensures that the loop has at least a 45° phase margin at the crossover frequency. Therefore, this zero should be placed close to the pole generated in the power stage which can be identified at frequency:

$$fP = \frac{1}{2p\,C_O R_{LOAD}}$$

where:

C_O = equivalent output capacitance of the error amplifier ≈120pF;

R_{LOAD}= load resistance.

The high frequency pole, fP2, can be placed at the output filter's ESR zero or at half the switching frequency. Placing the pole at this frequency will cut down on switching noise. The frequency of this pole is determined by the value of C_2 and R_1:

$$fP2 = \frac{1}{2p\,C_2 R_1}$$

One simple method to ensure adequate phase margin is to design the frequency response with a –20 dB per decade slope, until unity–gain crossover. The crossover frequency should be selected at the midpoint between f_{Z1} and f_{P2} where the phase margin is maximized.

V_{SW} Voltage Limit

In the boost topology, VSW pin maximum voltage is set by the maximum output voltage plus the output diode forward voltage. The diode forward voltage is typically 0.5 V for Schottky diodes and 0.8 V for ultrafast recovery diodes

$$V_{SW}(MAX) = V_{OUT}(MAX) + V_F$$

where:

V_F = output diode forward voltage.

In the flyback topology, peak V_{SW} voltage is governed by:

$$V_{SW}(MAX) = V_{CC}(MAX) + (V_{OUT} + V_F) \times N$$

where:

N = transformer turns ratio, primary over secondary.

When the power switch turns off, there exists a voltage spike superimposed on top of the steady–state voltage. Usually this voltage spike is caused by transformer leakage inductance charging stray capacitance between the VSW and PGND pins. To prevent the voltage at the VSW pin from exceeding the maximum rating, a transient voltage suppressor in series with a diode is paralleled with the primary windings. Another method of clamping switch voltage is to connect a transient voltage suppressor between the VSW pin and ground.

Magnetic Component Selection

When choosing a magnetic component, one must consider factors such as peak current, core and ferrite material, output voltage ripple, EMI, temperature range, physical size and cost. In boost circuits, the average inductor current is the product of output current and voltage gain

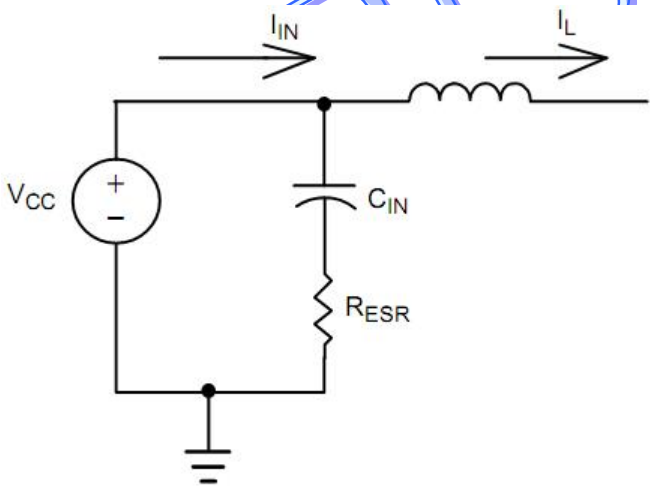
(VOUT/VCC), assuming 100% energy transfer efficiency. In continuous conduction mode, inductor ripple current is

$$I_{RIPPLE} = \frac{V_{CC}(V_{OUT} - V_{CC})}{(f)(L)(V_{OUT})}$$

where:

f = 280 kHz for HY5171. The peak inductor current is equal to average current plus half of the ripple current, which should not cause inductor saturation. The above equation can also be referenced when selecting the value of the inductor based on the tolerance of the ripple current in the circuits. Small ripple current provides the benefits of small input capacitors and greater output current capability. Core geometry like a rod or barrel is prone to generating high magnetic field radiation, but is relatively cheap and small. Other core geometries, such as toroids, provide a closed magnetic loop to prevent EMI.

Input Capacitor Selection



Boost Circuit Effective Input Filter

In boost circuits, the inductor becomes part of the input filter, as shown in figure "Boost Circuit Effective Input Filter". In continuous mode, the input current waveform is triangular and does not contain a large pulsed current. This reduces the requirements imposed on the input capacitor selection. During continuous conduction mode, the peak to peak inductor ripple current is given in the previous section. The product of the inductor current ripple and the input capacitor's effective series resistance (ESR) determine the VCC ripple. In most applications, input capacitors in the range of 10 µF to 100 µF with an ESR less than 0.3 Ω work well up to a full 1.5A switch current.

The situation is different in a flyback circuit. The input current is discontinuous and a significant pulsed current is seen by the input capacitors. Therefore, there are two requirements for capacitors in a flyback regulator: energy storage and filtering. To maintain a stable voltage supply to the chip, a storage capacitor larger than 20 µF with low ESR is required. To reduce the noise generated by the inductor, insert a 1.0 µF ceramic capacitor between VCC and ground as close as possible to the chip

Output Capacitor Selection

The output voltage ripple comes from two major sources, namely capacitor ESR and the charging/discharging of the output capacitor. In boost circuits, when the power switch turns off, I_L flows into the output capacitor causing an instant $\Delta V = I_{IN} \times ESR$. At the same time, current $I_L - I_{OUT}$ charges the capacitor and. increases the output voltage gradually. When the power switch is turned on, I_L is shunted to ground and I_{OUT} discharges the output capacitor. When the I_L ripple is small enough, IL can be treated as a constant and is equal to input current I_{IN}.

Summing up, the output voltage peak–peak ripple can be calculated by:

$$V_{OUT(RIPPLE)} = \frac{(I_{IN} - I_{OUT})(1-D)}{(f)(C_{OUT})} + \frac{I_{OUT} \times D}{(f)(C_{OUT})} + I_{IN} \times ESR$$

The equation can be expressed more conveniently in terms of VCC, V_{OUT} and I_{OUT} for design purposes as follows:

$$V_{OUT(RIPPLE)} = \frac{I_{OUT}(V_{OUT} - V_{CC})}{(f)(C_{OUT})} \times \frac{1}{(f)(C_{OUT})} + \frac{(I_{OUT})(V_{OUT})(ESR)}{(V_{CC})}$$

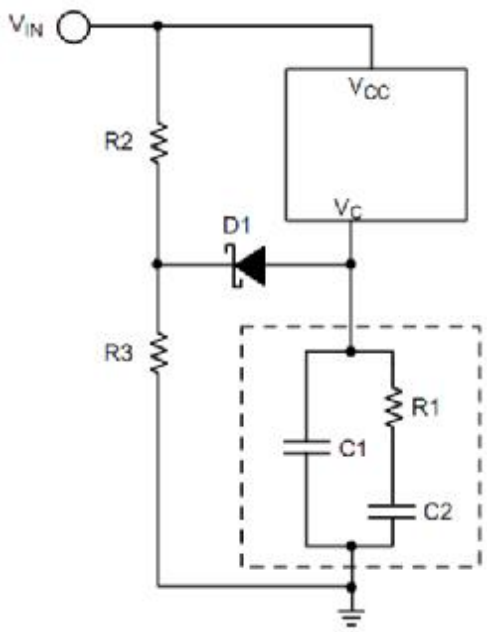
The capacitor RMS ripple current is:

$$I_{RIPPLE} = \sqrt{(I_{IN} - I_{OUT})^2 (1-D) + (I_{OUT})^2 (D)}$$

$$= I_{OUT} \sqrt{\frac{V_{OUT} - V_{CC}}{V_{CC}}}$$

Although the above equations apply only for boost circuits, similar equations can be derived for flyback circuits.

Reducing the Current Limit



Current Limiting with a Diode Clamp

In some applications, the designer may prefer a lower limit on the switch current than 1.5 A. An external shunt can be connected between the VC pin and ground to reduce its clamp voltage. Consequently, the current limit of the internal power transistor current is reduced from its nominal value.

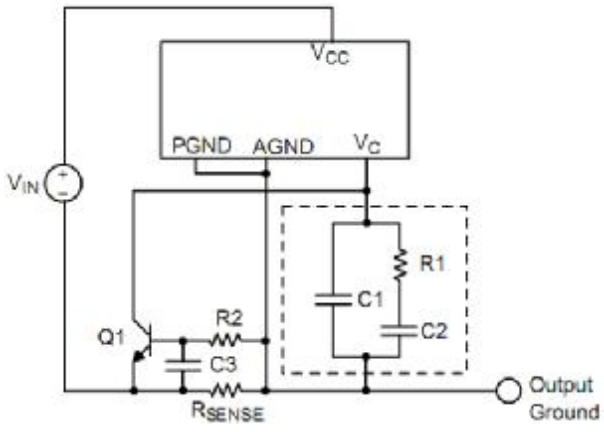
The voltage on the VC pin can be evaluated with the equation

$$V_C = I_{SW} \times R \times A_V$$

where:

R = 63mΩ, the internal emitter resistor;

A_V = 5 V/V, the gain of the current sense amplifier. Since R and A_V cannot be changed by the end user, the only available method for limiting switch current below 1.5A is to clamp the VC pin at a lower voltage. If the maximum switch or inductor current is substituted into the equation above, the desired clamp voltage will result. A simple diode clamp, as shown in above figure "Current Limiting with a Diode Clamp", clamps the VC voltage to a diode drop above the voltage on resistor R3. Unfortunately, such a simple circuit is not generally acceptable if VIN is loosely regulated.



Current Limiting with a Sense Resistor

Another solution to the current limiting problem is to externally measure the current through the switch using a sense resistor. Such a circuit is illustrated in figure "Current Limiting with a Sense Resistor".

The switch current is limited to

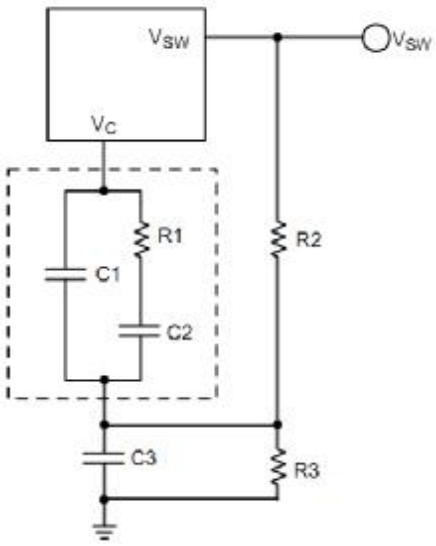
$$I_{SW(peak)} = \frac{V_{BE(Q1)}}{R_{SENSE}}$$

where:

$V_{BE(Q1)}$ = the base–emitter voltage drop of Q1.

The improved circuit does not require a regulated voltage to operate properly. Unfortunately, a price must be paid for this convenience in the overall efficiency of the circuit. The designer should note that the input and output grounds are no longer common. Also, the addition of the current sense resistor, R_{SENSE}, results in a considerable power loss which increases with the duty cycle. Resistor R_2 and capacitor C_3 form a low–pass filter to remove noise.

Sub-harmonic Oscillation



Technique for Increasing Slope Compensation

Sub-harmonic oscillation (SHM) is a problem found in current–mode control systems, where instability results when duty cycle exceeds 50%. SHM only occurs in switching regulators with a continuous inductor current. This instability is not harmful to the converter and usually does not affect the output voltage regulation. SHM will increase the radiated EM noise from the converter and can cause, under certain circumstances, the inductor to emit high–frequency audible noise. SHM is an easily remedied problem. The rising slope of the inductor current is supplemented with internal "slope compensation" to prevent any duty cycle instability from carrying through to the next switching cycle. In the HY5171, slope compensation is added during the entire switch on–time, typically in the amount of 180 mA/µs. In some cases, SHM can rear its ugly head despite the presence of the onboard slope compensation. The simple cure to this problem is more slope compensation to avoid the unwanted oscillation. In that case, an external circuit, shown in Figure "Technique for Increasing Slope Compensation", can be added to increase the amount of slope compensation used. This circuit requires only a few components and is "tacked on" to the compensation network

The dashed box contains the normal compensation circuitry to limit the bandwidth of the error amplifier. Resistors R2 and R3 form a voltage divider off of the VSW pin. In normal operation, VSW looks similar to a square wave, and is dependent on the converter topology. Formulas for calculating VSW in the boost and flyback topologies are given in the section "VSW

Voltage Limit." The voltage on VSW charges capacitor C3 when the switch is off, causing the voltage at the VC pin to shift upwards. When the switch turns on, C3 discharges through R3, producing a negative slope at the VC pin. This negative slope provides the slope compensation.

The amount of slope compensation added by this circuit is

$$\frac{\Delta I}{\Delta T} = VSW\left(\frac{R_3}{R_2+R_3}\right)\times\left(1-e^{\frac{-(1-D)}{R_3C_3 f_{SW}}}\right)\times\left(\frac{f_{SW}}{(1-D)\times R\times AV}\right)$$

where:

ΔI/ΔT = the amount of slope compensation added (A/s);

VSW = the voltage at the switch node when the transistors turned off (V);

f_{SW} = the switching frequency, typically 280 kHz

D = the duty cycle;

R =63m Ω, the value of the internal emitter resistor;

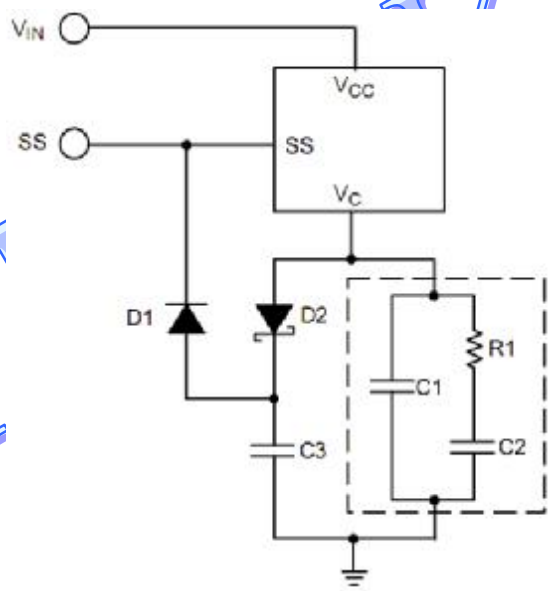
AV = 5 V/V, the gain of the current sense amplifier.

In selecting appropriate values for the slope compensation network, the designer is advised to choose a convenient capacitor, and then select values for R2 and R3 such that the amount of slope compensation added is 100 mA/μs. Then R2 may be increased or decreased as necessary. Of course, the series combination of R2 and R3 should be large enough to avoid drawing excessive current from VSW. Additionally, to ensure that the control loop stability is improved, the time constant formed by the additional components should be chosen such that

$$R_3C_3 < \frac{1-D}{f_{SW}}$$

Finally, it is worth mentioning that the added slope compensation is a trade–off between duty cycle stability and transient response. The more slope compensation a designer adds, the slower the transient response will be, due to the external circuitry interfering with the proper operation of the error amplifier.

Soft Start



Soft Start

Through the addition of an external circuit, a soft–start function can be added to the HY5171 of components. Soft–start circuitry prevents the VC pin from slamming high during startup, thereby inhibiting the inductor current from rising at a high slope. This circuit, shown in Figure "Soft Start", requires a minimum number of components and allows the soft–start circuitry to activate any time the SS pin is used to restart the converter.

Resistor R1 and capacitors C1 and C2 form

the compensation network. At turn on, the voltage at the VC pin starts to come up, charging capacitor C3 through Schottky diode D2, clamping the voltage at the VC pin such that switching begins when VC reaches the VC threshold, typically 1.05 V.

$$VC = V_{F(D2)}+V_{C3}$$

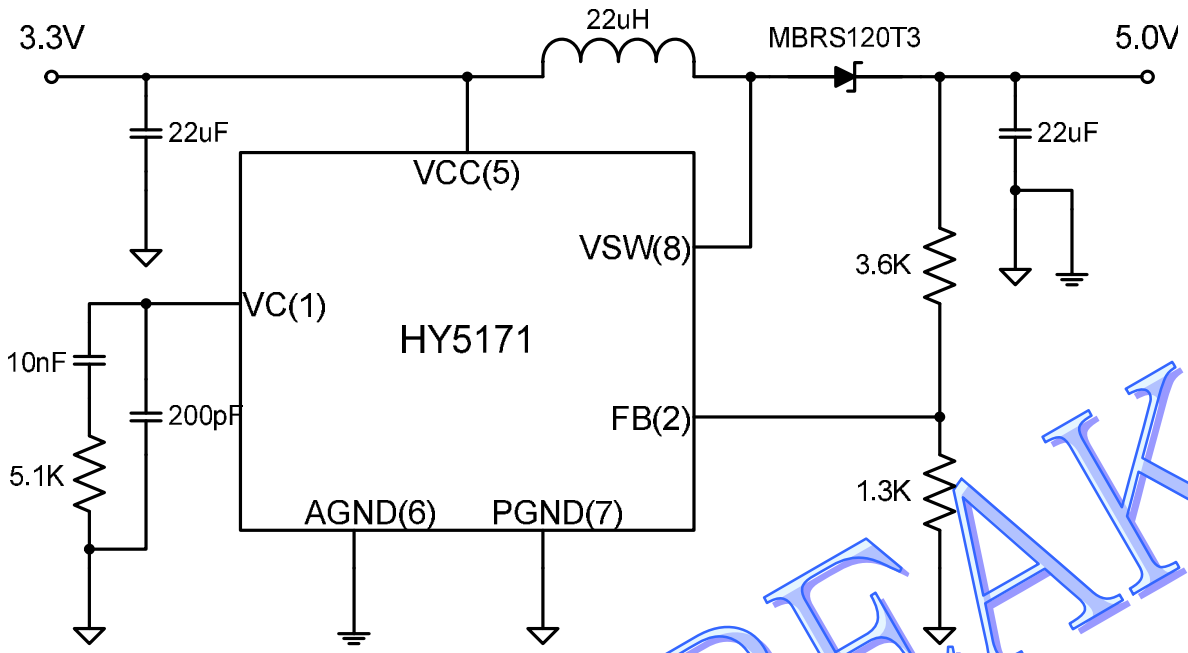
Therefore, C3 slows the startup of the circuit by limiting the voltage on the VC pin. The soft–start time increases with the size of C3. Diode D1 discharges C3 when SS is low. If the shutdown function is not used with this part, the cathode of D1 should be connected to VIN.

Circuit Layout Guidelines

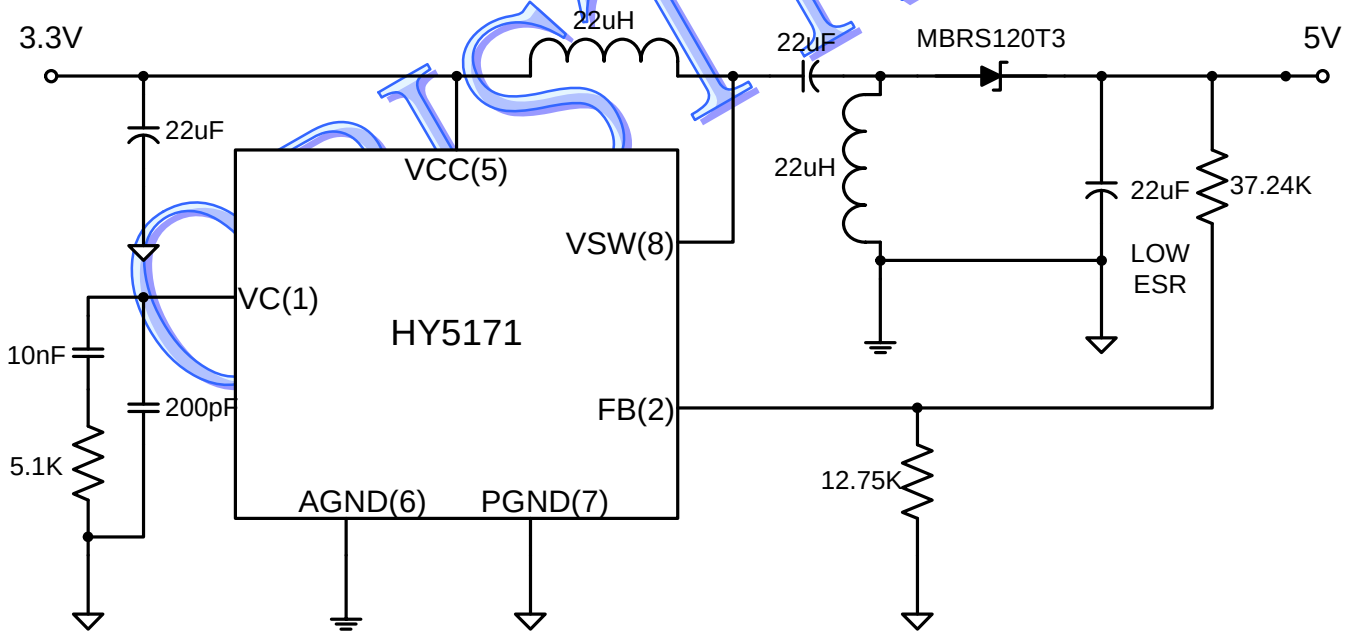
In any switching power supply, circuit layout is very important for proper operation. Rapidly switching currents combined with trace inductance generates voltage transitions that can cause problems. Therefore the following guidelines should be followed in the layout.

1. In boost circuits, high AC current circulates within the loop composed of the diode, output capacitor, and on–chip power transistor. The length of associated traces and leads should be kept as short as possible. In the flyback circuit, high AC current loops exist on both sides of the transformer. On the primary side, the loop consists of the input capacitor, transformer, and on–chip power transistor, while the transformer, rectifier diodes, and output capacitors form another loop on the secondary side. Just as in the boost circuit, all traces and leads containing large AC currents should be kept short.
2. Separate the low current signal grounds from the power grounds. Use single point grounding or ground plane construction for the best results.
3. Locate the voltage feedback resistors as near the IC as possible to keep the sensitive feedback wiring short. Connect feedback resistors to the low current analog ground.

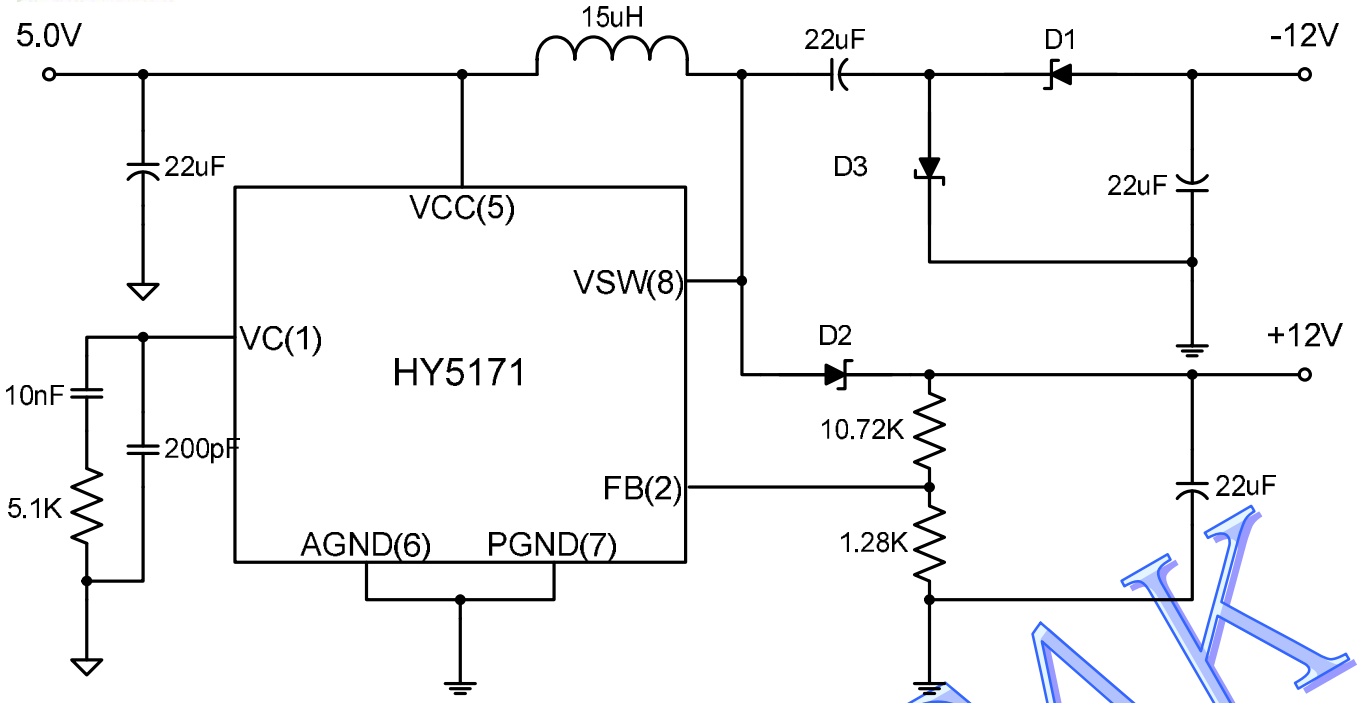
ADDITIONAL APPLICATION DIAGRAM



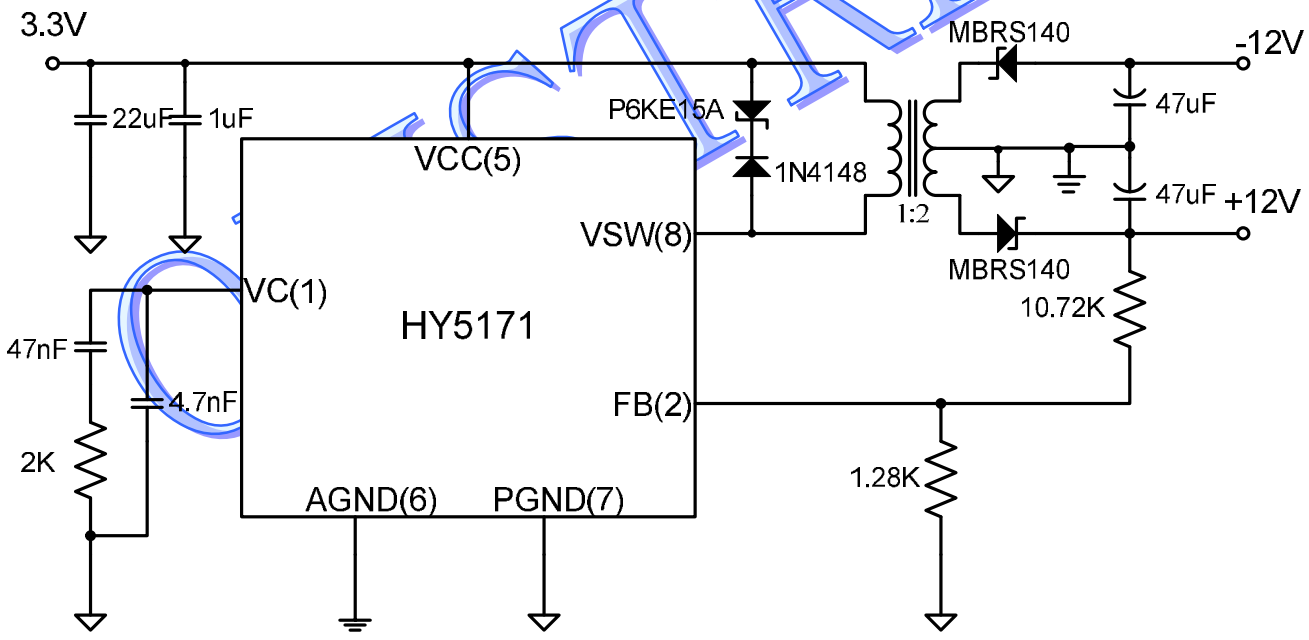
3.3V Input, 5.0V / 400mA Output Boost Converter



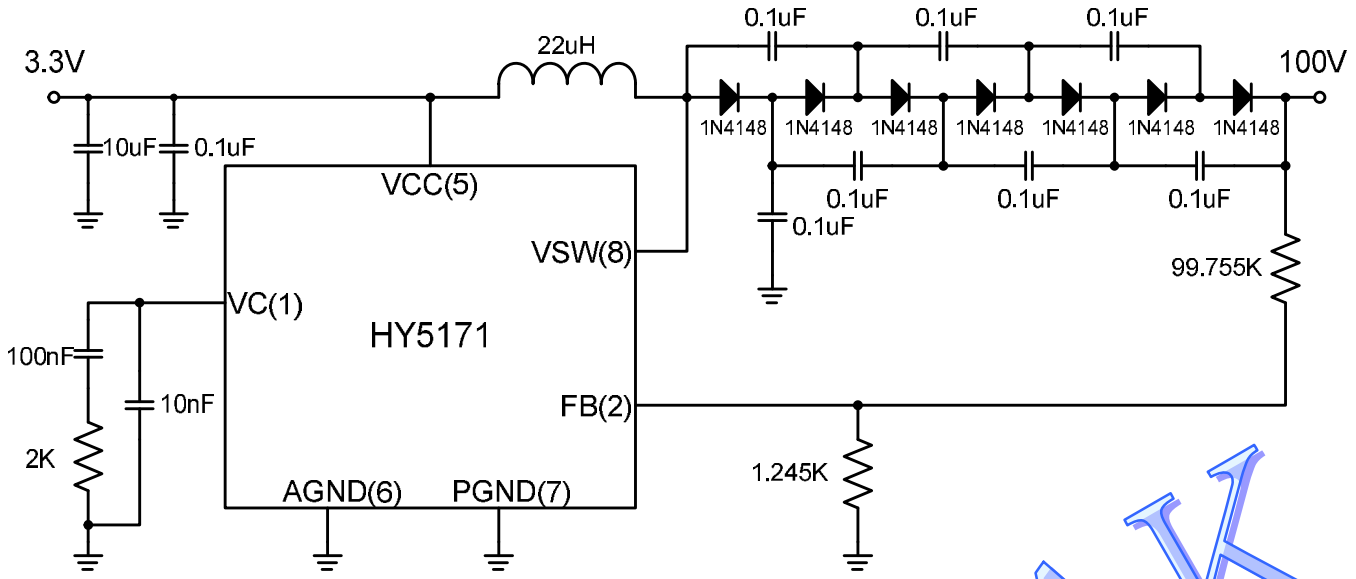
2.7V to 28V Input, 5.0V Output SEPIC Converter



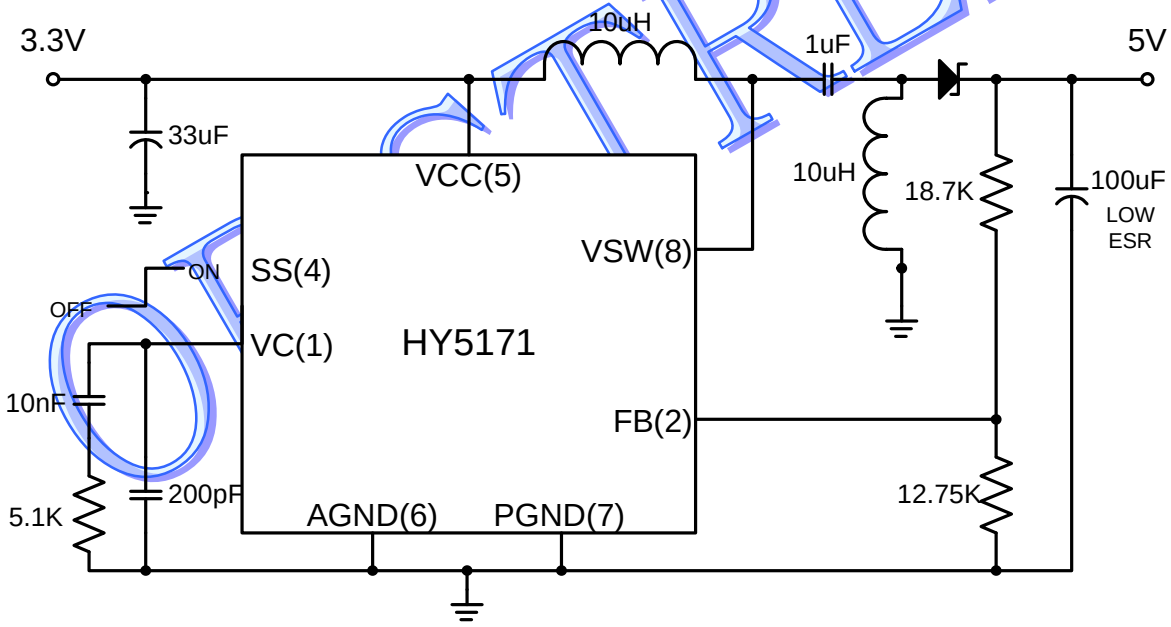
5.0V Input, 12V Output Dual Boost Converter



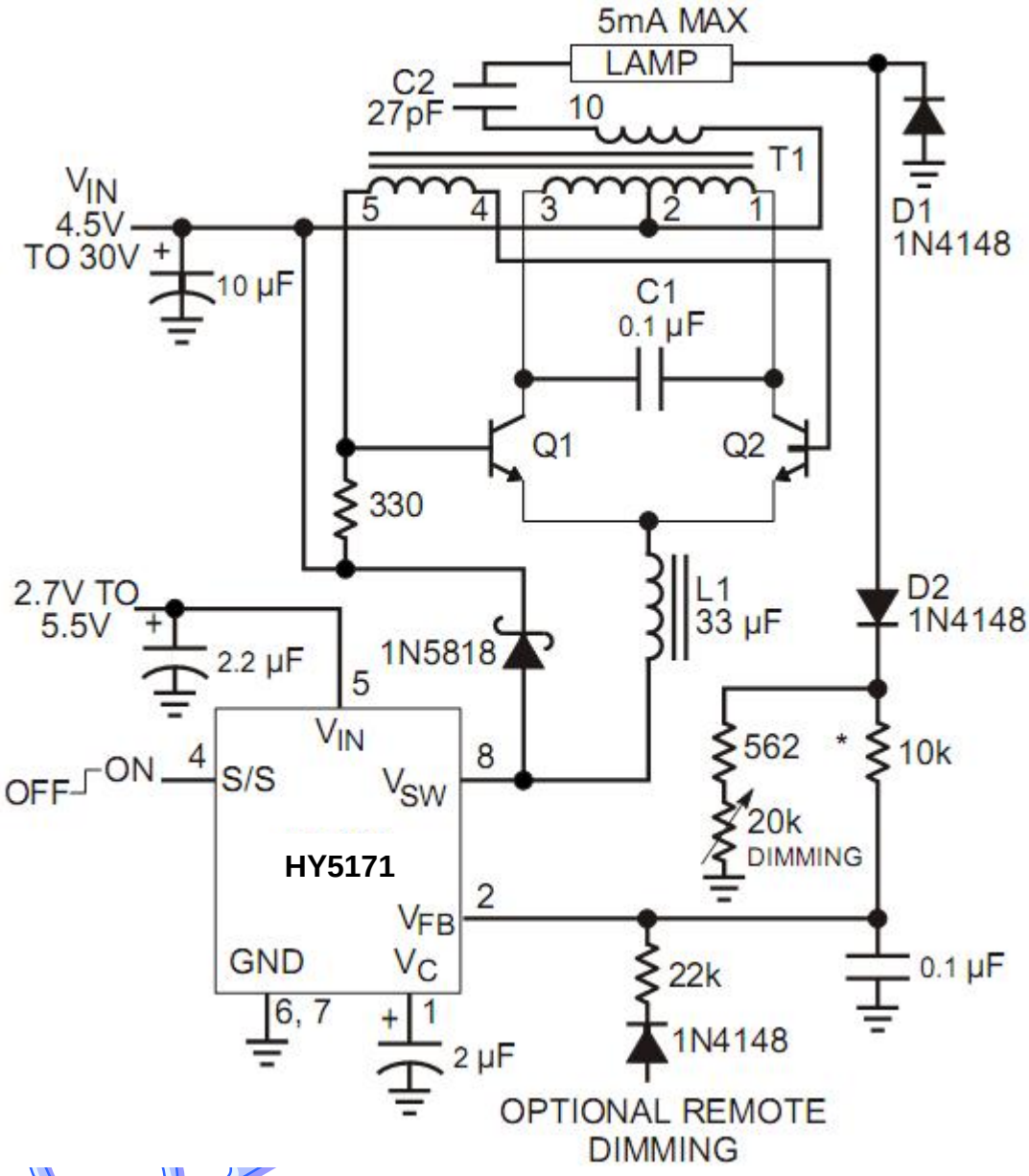
2.7V to 13V Input, 12V/200mA Output Flyback Converter



4.0V Input, 100V/10mA Output Boost Converter

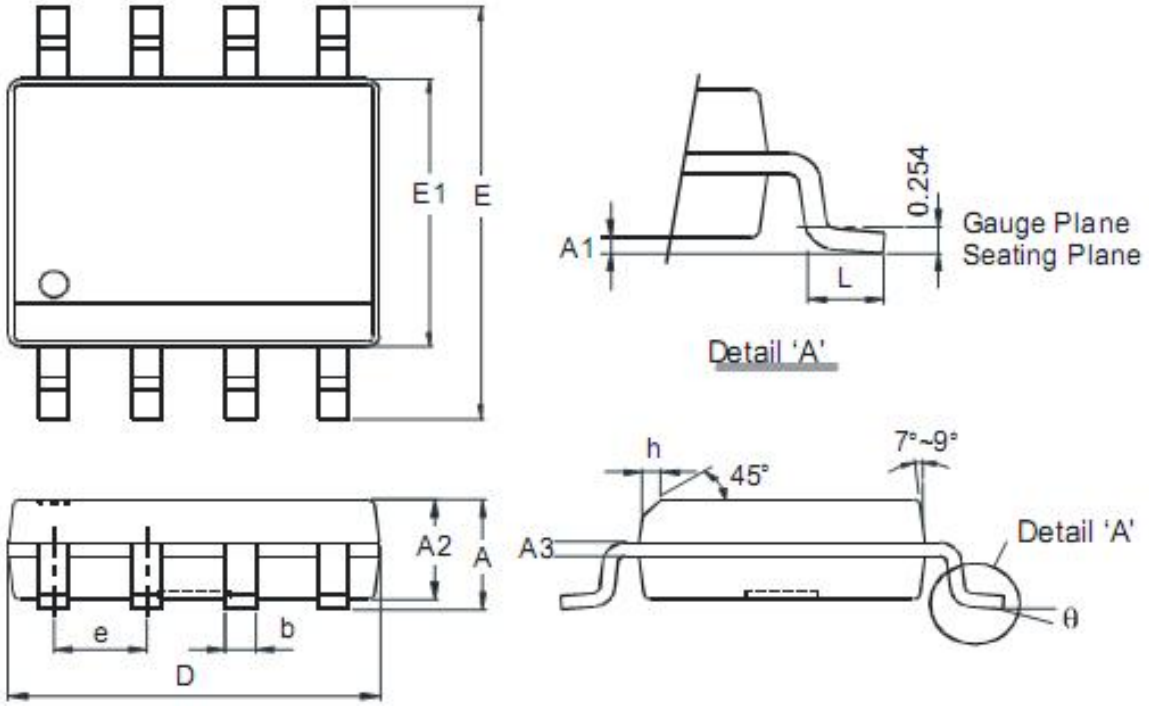


Li-Lion Cell t0 5V Output SEPIC Converter



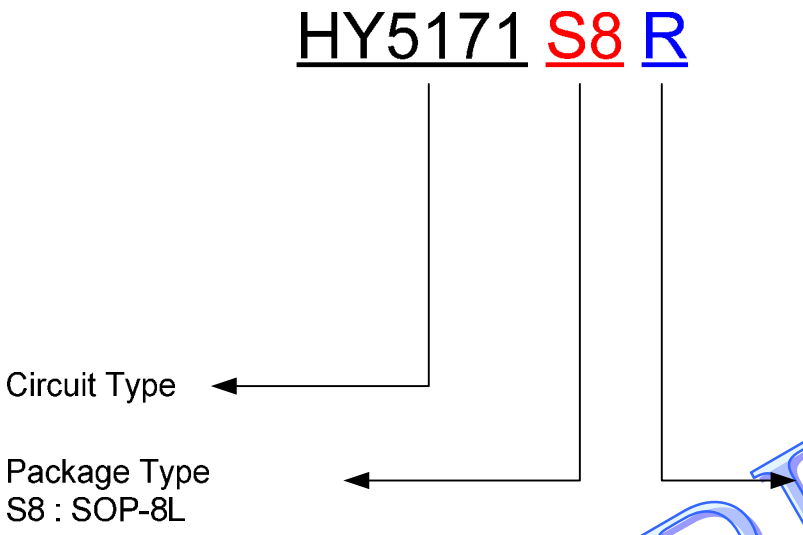
CCFL Supply

Package Outline Dimensions



SOP-8L		
Dim	Min	Max
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

ORDERING INFORMATION



ORDERING REMEMBER	OUTPUT VOLTAGE	PACKAGE	SHIPPING
HY5171S8R	N/A	SOP-8L	3,000 Units/ Tape & Reel